Basics of Low Noise Amplifier Design

A number of important design requirements must be considering when undertaking the development of a high performance low noise amplifier (LNA) including:

1) Noise Figure (NF)
2) Input 1 dB compression point (P1dB)
3) Input second and third order intercept (IIP2 and IIP3)
4) Gain
5) DC power
6) Bandwidth (BW)
7) Frequency of operation (narrowband or broadband)
8) S-parameters/matching
9) Survivability

All of the above parameters will impact the LNA architecture and resultant performance. In general, the process technology must be selected to permit achievement of required specifications. Typically, a SiGE or BiCMOS process is chosen where low noise is an important consideration because bipolar devices will offer the lowest noise performance.

Architectural approaches include active and passive matching for the input and output 50 Ω match. Passive matching is based on an open loop LNA design, while active matching is based on feedback. Common emitter (source) or common base (gate) approaches are part of the consideration to meet the overall LNA specifications. The common base and common emitter architectures have inherent trade-offs between the two approaches for noise, gain, BW, and IP3. The final selection of the LNA topology must take into account the rest of the receiver performance after the LNA. Thus, the block specifications for the LNA are typically derived from the overall receiver link budget. This budget defines the LNA gain, bandwidth, NF, P1dB, IP2, IP3, and DC power. This link budget is an important part of the design process, as performance limitations of the LNA will be traded off with performance of other blocks in the receiver. A set of specifications for the LNA can be defined based on the parameters above. This LNA block level requirement can be used to perform a transistor level circuit architecture trade-off study through circuit simulation using SpectreRF, Eldo RF, or any circuit simulation tool that supports of the selected process. The circuit simulations are performed to determine, based on the defined specification, which LNA architecture is appropriate in order to meet the overall LNA specifications. The circuit simulations provide the integrated circuit (IC) design team insight into the transistor level circuit architectures that support the overall LNA specification. The circuit architecture simulation study is used to confirm the LNA architectural approach.

Depending on single-ended versus differential LNA topologies, parameters such as power supply rejection (PSRR) and IP2 will be parameters to be concerned about for the LNA design. In order to reduce the noise of the LNA, a typical approach is to increase the device size. The increase in capacitance as a result of the noise reduction can cause bandwidth and IP3 reduction. Circuit techniques can be used, such as bootstrapping, to enhance both of these performance parameters. Thus, it is possible, depending on the frequency of operation, to have low noise, wide bandwidth, and high IP3.

The LNA IC designer will take the input and output loading of the LNA into consideration. In the case of external matching, the input and output interface for the LNA, usually 50 Ω, will cause the DC power of the LNA to be higher. This is a result of the fact that the LNA output must match and drive 50 Ω. If the LNA output remains on-chip, as part of an integrated receiver, then the LNA output could drive a high impedance load, and this would help to reduce the DC power requirement. The LNA top level schematic must be assembled and verified through simulation. The top-level schematic will include biasing, decoupling, input and output blocking capacitors, ESD, power supply clamps, and any other circuitry required for the LNA IC.

If the LNA is part of an integrated receiver, it is possible to use either a single-ended input common base (gate) or common emitter (source) input stage to perform single-ended-to-differential conversion on-chip. This will allow the input to the next stage in the on-chip receiver to be differential.

The LNA schematic design can be simulated to determine the sensitivity of the design to process, voltage, and temperature (PVT). This set of simulations is performed to verify that the base line LNA design is sound. In order to simulate the impact on mismatch on the LNA, Monte Carlo (MC) mismatch simulations should be performed. This battery of simulations will provide insight to the sensitivity of the LNA performance, as well as the overall LNA performance, to mismatch. As part of the LNA design process, once the first version of the top level LNA layout is completed, parasitic extraction (PEX) simulations must be completed. Included in these simulations is a model for the intended package for the LNA IC. The PVT and MC mismatch simulations described above are performed at the schematic level. Once the first version of the LNA layout is completed, the layout is extracted and simulated. If it is determined that the performance has degraded, the layout must be optimized ideally to the point where the block level performance extracted does not degrade from the schematic view. Once the layout has been optimized, the layout is extracted again to verify that the top level LNA layout meets all of the specifications. The amount of time required for the optimization of the layout, and associated simulations to verify, can potentially be on the order of, or longer than, the time required for the schematic design effort. The reason for this is simple. As the frequency of operation increases, the layout and package parasitics have a much greater impact on the performance of the LNA.

If the LNA is an intellectual property (IP) block to be used in a larger RF Transceiver or on a System-On-A-Chip (SOC), consideration is required for the noise and spurious content that will be present on the power supplies. Also, the input and output loading must be taken into account. These issues must be included as part of the LNA design methodology for inclusion in the simulation list for the block and top level LNA simulations. Built-In-Self-Test (BIST) or testability visibility for the LNA must also be thought about in the context of an RF Transceiver, or a SOC, and an approach to look at the performance of the LNA block individually must be determined during prototype and production testing.