Design Challenges of Analog-To-Digital Converters (ADC)

There are a number of design challenges and considerations when undertaking the development of an ADC. The ADC architectural approach and choice of the integrated circuit process are influenced by the input signal swing, ADC sample rate, the ADC effective number of bits (ENOB), the DC power consumption, available power supplies, the ADC latency (the delay time for sampling and digitizing the analog input signal), the ADC instantaneous bandwidth (IBW), differential nonlinearity (DNL), integral nonlinearity (INL), and the spur free dynamic range (SFDR).

The first step in the process is select the appropriate ADC type. Typically, the experienced design engineer can select one or two candidates for the type of converter to implement based on the overall requirements. The most common ADC types include flash, successive approximation register (SAR), pipeline, dual slope, and sigma-delta. There are variations within each grouping.

Once the type of converter is determined, the top-level ADC specification can be used to define circuit block level requirements based on the desired ADC architecture. These block level requirements can be used to perform several different types of analysis. The first type of analysis is simple hand calculations, based on the process development kit (PDK), for such parameters as resistor, capacitor, and transistor matching. A powerful analysis type is to development a behavioral model of the ADC, using either Verilog-A, MATLAB, or Simulink. This will allow very rapid analyses of various architectural permutations. The third type of analysis are simulations at the transistor level, using Spectre, Eldo, or any circuit simulation tool that supports the selected process. These analyses are performed to determine, based on the identified circuit blocks, which ADC architecture is appropriate in order to meet the ADC specifications. The circuit simulations provide the integrated circuit (IC) design team insight into the transistor level circuit architectures that support the overall ADC specification.

Once the ADC architecture has been determined, the overall ADC specification can be broken down into a block level budget with requirements for DC linearity, SFDR (in terms of single tone harmonic distortion (HD) and two tone intermodulation (IM) products), thermal noise, settling time (time it takes to settle to an accuracy of N bits of the final value), DC power, AC bandwidth, gain, power supply rejection (PSRR) for all of the blocks in the ADC. The ADC IC design team will then design the ADC blocks, taking input and output loading of each block into consideration. These parameters will pose design challenges and trade-offs for the design team during the design phase of the ADC.

Once each of the ADC blocks is completed, the ADC top level schematic must be assembled and verified through simulation. For verification of DNL and INL, a slow input ramp, varying from minus full scale (FS) to plus full scale (+/- FS) can be used. A Verilog-A model of a digital-to-analog converter (DAC) can be used to take the ADC digital output bits and convert back to an analog signal. The analog output is a reconstruction of the analog input signal to the ADC. The analog output signal can be used to look at the DNL for code-to-code transitions. The analog output waveform can also be used to do a least-squares fit (LSF) of the overall ADC transfer function to look at INL. This is accomplished by taking a sample of the analog signal at the end of each step out of the Verilog-A DAC and doing an LSF to the resulting transfer function in order to look at the overall INL for the ADC. The HD and IM performance of the ADC can be determined

in simulation by using a single tone or two tone sine wave input signal. The Verilog-A DAC output can be put through a Fast Fourier Transform (FFT), and the harmonics and intermodulation products can be determined. It should be noted that the proper number of time samples are needed, and the appropriate FFT windowing is required in order to obtain correct results. The nominal performance of the ADC can be simulated over process, voltage, and temperature (PVT) in order to verify that the base line ADC performance does not degrade over power supply variations, process corners, and temperature. This battery of simulations will verify that the base line ADC design is sound.

Also, on-chip voltage references must be implemented. Using off-chip reference circuitry will introduce extra parastics in the form of inductance which will cause the reference voltages to degrade the settling performance of the converter. The extra movement of the reference voltages will degrade the overall ENOB of the chip due to this settling error introduced by the off-chip reference.

In addition to on-chip references, there must be enough on-chip and off-chip decoupling on the power supplies in order to guarantee performance. Using supplies that vary too much due to switching noise and switching spurs can also limit the ENOB of the ADC.

One consideration for an ADC resolution specification is the limitation of matching for an IC process. If the resolution of the ADC specification is beyond what is physically possible in an IC process, then the INL and DNL of the ADC must be trimmed in order to achieve the overall specification. There are many well documented approaches to trimming an ADC. Based on the approach chosen, it may be necessary to store the trims on-chip in some form of non-volatile (NV) memory. Digital bits are used to adjust the values of the parameters that are being changed to correct for the impact of finite device mismatch in the ADC. These bits are then stored in the on-chip NV memory. The bits for the trims can be determined at wafer test or packaged test. If the trims are determined at one temperature only, the ADC performance must be measured over temperature to verify that the trims used can maintain performance over temperature. If this is not the case, then it may be necessary to have a temperature sensor on-chip that determines the junction temperature of the chip, and point to a trim look-up table that's a function of temperature. In order to simulate the impact on mismatch on the ADC design, Monte Carlo (MC) mismatch simulations should be performed. This battery of simulations will provide insight to the magnitude of the resultant ADC errors due to mismatch, as well as provide insight into the amount of trim range needed, based on the trim approach. For each MC case, several simulations must be performed. The first simulation result will show the untrimmed performance of the ADC. The trims for the ADC must then be adjusted, in simulation, in order to correct for the mismatch errors, and then re-simulated in order to conform the performance. This can be a painstakingly long process, as each trim must be adjusted and re-simulated multiple times in order to verify that the trim is properly correcting for the mismatch errors.

Another on-chip feature to consider is analog or digital dither. Based on the ADC specification, dither can be used to help the ADC meet the DNL requirement. Depending on a number of factors, dither can be used to help to randomize some of the ADC errors. Since energy is conserved, the RMS power of the dithered spurs is transferred to the ADC noise floor, and is spread across the

entire Nyquist region. There are a number of different implementations of dither, and each approach to dither impacts the overall ADC transfer function and performance differently. In order to simulate the impact of dither on the ADC performance, a transient noise simulation is required, and an FFT must be performed on the Verilog-A DAC output waveform with and without the inclusion of the dither.

As part of the ADC design process, once the first version of the top level ADC layout is completed, parasitic extraction (PEX) simulations must be completed. Included in these simulations is a model for the intended package for the ADC IC. The PVT and MC mismatch simulations described above are performed at the schematic level. Once the first version of the ADC layout is completed, the individual block layouts are extracted and simulated. If it is determined that the performance has degraded, the layout must be optimized ideally to the point where the block level performance extracted does not degrade from the schematic view. Once all of the block layouts have been optimized, this approach is then repeated at the ADC top level. The amount of time required for the optimization of the layout, and associated simulations to verify, can potentially be on the order of the time required for the schematic design effort.

If the ADC is an intellectual property (IP) block to be used in a larger System-On-A-Chip (SOC), consideration is required for the noise and spurious content that will be present on the power supplies. Also, input and output loading must be taken into account. These issues must be included as part of the ADC design methodology for inclusion in the simulation list for the block and top-level ADC simulations. Built-In-Self-Test (BIST) or testability visibility for the ADC must be considered and an approach to look at the performance of the ADC block individually must be determined during prototype and production test.