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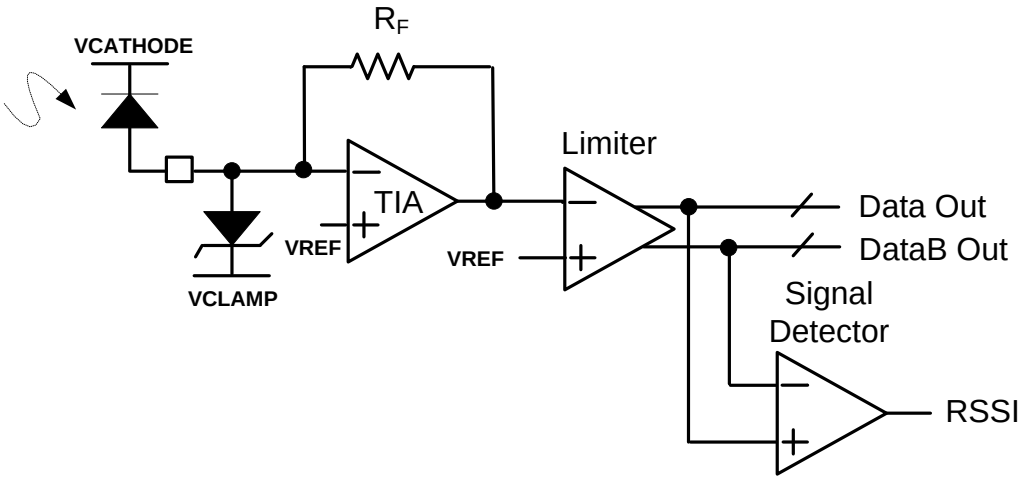
LM-HSTIA-01 Low Noise, Wideband TIA IP Block

Introduction

This document describes the features and key specifications of a Low Noise, Wideband TIA IP block. The process technology for this block is 180 nm SiGe. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- 28 Gbps operation
- 4 channel version supports 100 GBps
- TIA / Limiter / RSSI stages with 100Ω differential load
- 6 KΩ Transimpedance Gain with > 20 GHz BW
- Average power < 40 mW per channel
- Input peak current signal > 3 mA
- Input referred noise: 510 nA RMS over 20 GHz BW
- 120 mV differential output voltage swing (minimum)



Deliverables:

- Verilog Model
- LIB (best/worst) & LEF models
- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-HSTIA-01	180 nm SiGe	0 to 70C	1