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LM-LPSD-ADC-01

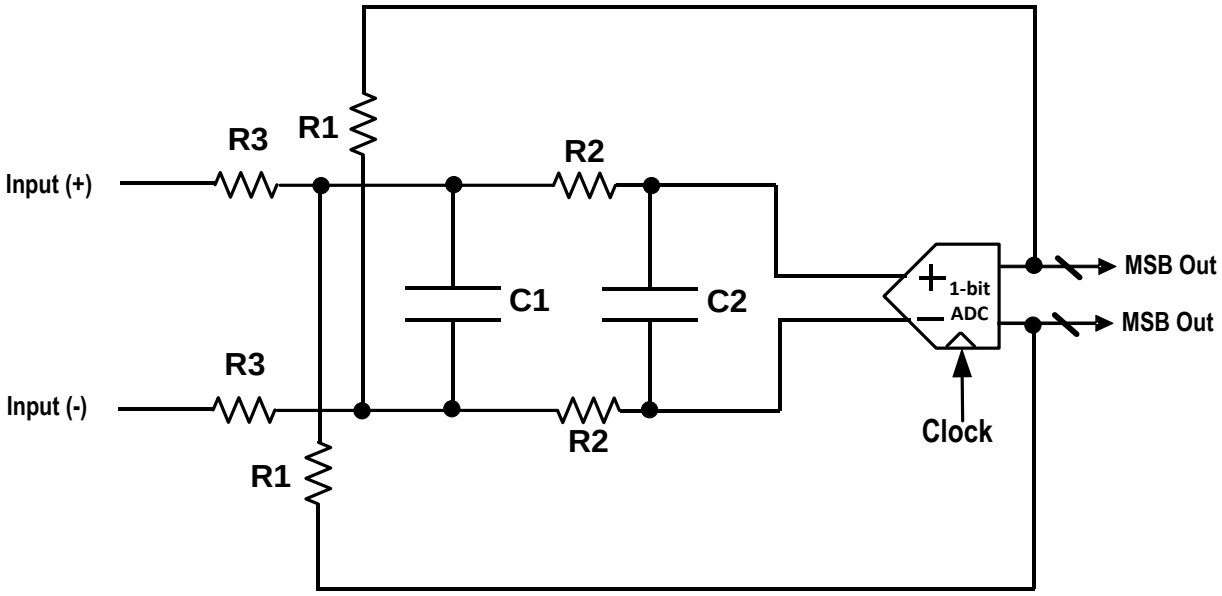
Low Power Σ-Δ ADC IP Block

Introduction

This document describes the features and key specifications of a Low Power ΣΔ ADC IP block. The process technology for this block is 180 nm CMOS. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- Second Order, 1 bit modulator
- Resolution: 6.5 bits
- Maximum input frequency 50 kHz
- ADC clock input frequency: 24 MHz nominal
- Full scale input: 1.25V peak-to-peak single-ended
- Noise density @ 100 KHz, 55 dB, FS, @ 1 MHz, 40 dB, FS
- SNR @ 50 KHz, -2 dB, FS input, > 55 dB, FS
- SFDR @ 50 KHz, -2 dB, FS input, > 46 dB, FS
- 1.8V power supply, 1.5 mW



Deliverables:

- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-LPSD-ADC-01	180nm CMOS	0 to 70C	1