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LM-PLL-30001-01 Wideband Phase-Locked Loop IP Block

Introduction

This document describes the features and key specifications of a Wideband Phase-Locked Loop (PLL) IP block. The process technology for this block is 180 nm CMOS. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- Selectable clock inputs: 10 MHz or 20 MHz nom
- Output frequencies: 600 to 925 MHz or 300 to 462.5 MHz
- Programmable S and P counters
- Active power 34 mA or less

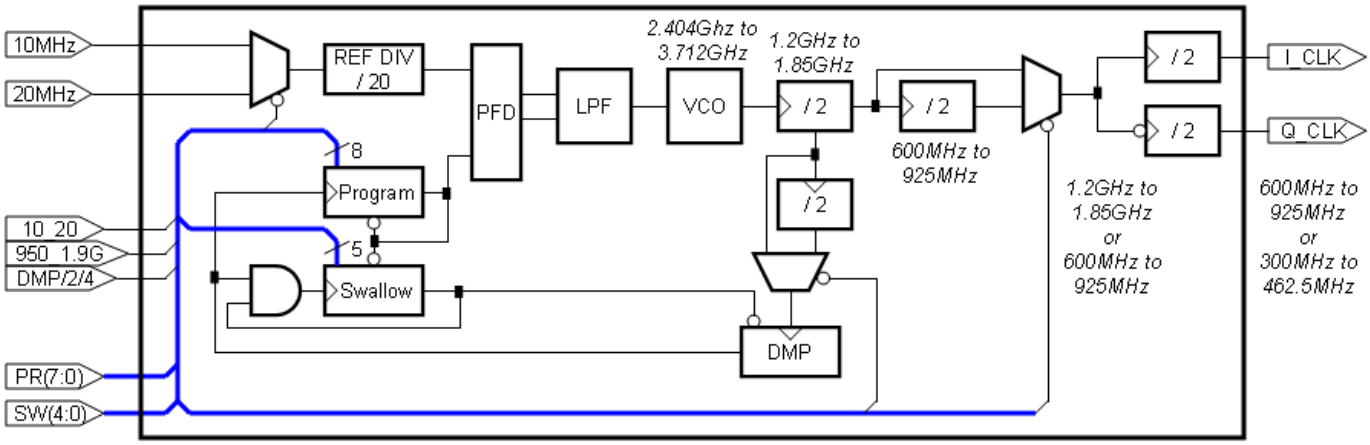

Figure 1: Circuit Diagram

Deliverables:

- Verilog Model
- LIB (best/worst) & LEF models
- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-PLL-30001-01	180 nm CMOS	0 to 70C	1