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LM-PLL-30002-01

RF Phase-Locked Loop IP Block

Introduction

This document describes the features and key specifications of a RF Phase-Locked Loop (PLL) IP block. The process technology for this block is 180 nm CMOS. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- Wide frequency input range: 10 MHz to 80 MHz
- Output frequency: 2.5 GHz @ 80 MHz FREF
- Active power 20 mA or less
- Standby down to 1 μ A

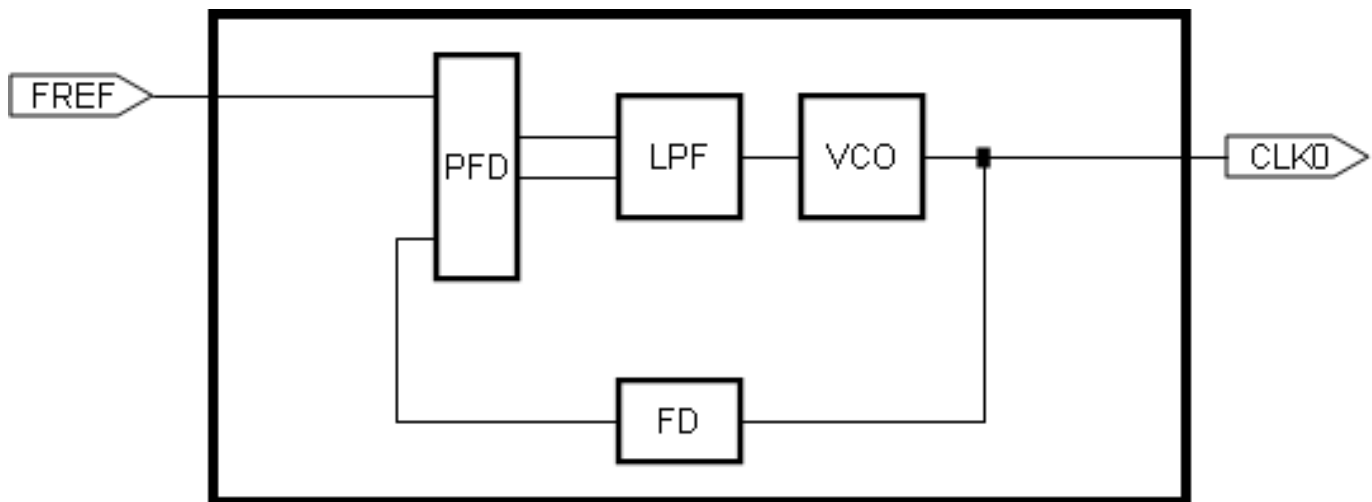


Figure 1: Circuit Diagram

Deliverables:

- Verilog Model
- LIB (best/worst) & LEF models
- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-PLL-30002-01	180 nm CMOS	0 to 70C	1