Linear Microsystems, Inc.
14 Goodyear, Suite 135
Irvine, CA 92618
(949) 273-5473 ph
(949) 273-5607 fax

LM-PLL-30003-01 Wideband, RF Phase-Locked Loop IP Block

Introduction

This document describes the features and key specifications of a Wideband, RF Phase-Locked Loop (PLL) IP block. The process technology for this block is 180 nm CMOS. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- Wide frequency input range: 10 MHz to 120 MHz
- Wide frequency output range: 10 MHz to 1.5 GHz
- Automatic Lock and output control
- 2 outputs – post VCO and post Output Divider
- Standby down to 1 µA
- Active power 20 mA or less
- Output enable and internal frequency dividers programmable through internal control block.

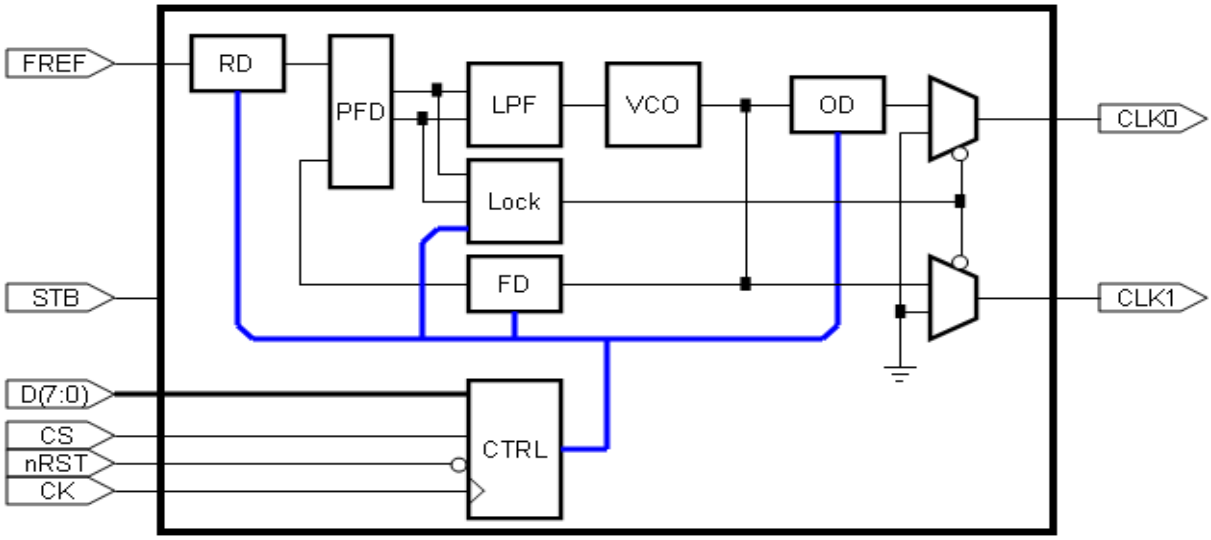

Figure 1: Circuit Diagram

Deliverables:

- Verilog Model
- LIB (best/worst) & LEF models
- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-PLL-30003-01	180 nm CMOS	0 to 70C	1