RF ASIC Design – Considerations and Challenges

The development of a RF ASIC involves a set of challenges beyond those encountered doing baseband IC design. First and foremost is the demand that a RF ASIC puts on process technology. Beyond fast transistors, high performance passives are needed that have minimal parasitics to minimize bandwidth reduction and crosstalk. Often, there is a need for high Q inductors in the process. Typically, the performance specifications of RF ASICs drive implementation into either SiGe or deep submicron processes, optimized for RF performance. Also, development time is longer because extensive simulations are needed to consider all the effects of parasitics and some electrical/physical design iteration is necessary to account for layout parasitics. Therefore, RF ASICs usually require a larger NRE budget due to the process constraints and amount of needed engineering resources.

The testing of RF ASICs is also a challenge, especially at the wafer level. Often RF ASICs are sold in die form since they are part of a type of a MCM or chip-on-board packaging technology. In these cases, wafer testing must occur at RF frequencies. This often requires special probe cards and prober hardware and requires the knowledge of a test team with RF background. A common package for RF ASICs is a QFN package since the paddle can act as a ground plane. The tester interface hardware must be carefully designed and fabricated to minimize the effect of stray parasitics and mismatch on the measurements.

As part of the process in selecting a suitable process technology, the design team must choose the appropriate architecture and arrive a reasonable set of requirements that matches not only the product requirements, but that can be implemented in the target budget and schedule. In a RF ASIC, it may be necessary to conduct an investigation phase of 2-6 weeks in concert with the customer to arrive at a satisfactory project plan.

In this investigation phase, some of the major design parameters for considerations include:

1) DC power/available power supplies
2) Half or full duplex operation
3) Receive and transmit frequencies and instantaneous Bandwidth (IBW)
4) Receiver input transmitter output dynamic range
5) Receiver and transmitter Frequency planning
6) On / off-chip filtering
7) Number of channels
8) Channel-to-channel isolation
9) On/off-chip PLL and VCO pulling due to Power Amp (PA)
10) DC power dissipation
11) Receiver sensitivity/Transmitter power, peak-to-average ratio (PAR), and efficiency
12) Image noise
13) LO feed-through (fundamental, second harmonic, and IM products) and offset trims for reduction
14) Attenuation/automatic gain control (AGC)
15) Impact of ESD

The RF ASIC architectural approach and choice of the integrated circuit process are significantly impacted by these parameters.

An experienced RF design engineer will consider all of these factors and create a link budget that is used to develop specs for individual circuit blocks in the ASIC. Typically, the ASIC team will have a lead architect reasponsible for this overall link budget and specifications. This link budget will consider factors such as noise figure (NF), gain, second order intercept (IP2), third order intercept (IP3), compression point (P1dB), and bandwidth. Depending on single-ended versus differential RF topologies, parameters such as power supply rejection (PSRR) and IP2 must be considered.

Due to the complexity of RF ASICs, a design team typically consists of multiple design engineers to design various parts of the chip. For example, in a complex ASIC or SoC, a RF direct conversion receiver could consist of a low noise front end, down converter and demodulator, a high performance ADC, a PLL, and digital signal processing (DSP). Each of these blocks could require one or several engineers working in concert.

Besides a detailed block design, the lead architect will be responsible to develop an approach for system level simulation to model the overall predicted performance to the requirements using mixed-signal simulation along with some behavioral level modeling of the system. Often, a degree of design iteration is necessary of the individual blocks to reach the desired performance level at the top level of the RF ASIC.

Typically, RF block design requires extensive simulations over PVT and requires Monte Carlo analysis as well since the performance at the highest frequencies are very dependent on model parameter variations and the effect of parasitics. The effects of layout parasitics must be considered. Adequate time must be allowed in the schedule for extensive simulation time, parasitic extraction and electrical/physical design iteration.

In designs with both a transmit and receive path, one approach is to have the design team focus on the design the receiver blocks first, and then reuse the designed blocks in reverse as a base line design for the transmitter. This could save a significant amount of design time and development money.

An advantage of integrated RF design is the large degree of freedom in specifying inter-block impedances. There is no need to keep to a 50 Ω system which can save a significant amount of power. It is best to develop architectures that can make use of the available passive components of the process. In some cases, it could necessary to go off-chip for filtering. Also, typically the I/O requires matching to 50 Ω; the modeling of the package and board parasitics must be considered in these cases.

Often the RF circuitry can be part of a larger SoC (system-on-a-chip) where considerations of noise immunity and crosstalk are important. Careful consideration must be given to the overall physical layout of the chip and great care must be given to the power supply routing scheme and the number and location of the power and grounds.

There are good solutions to all of the design considerations as well as process and testing requirements that are offered by ASIC companies with extensive RF expertise, such as Linear MicroSystems, Inc.