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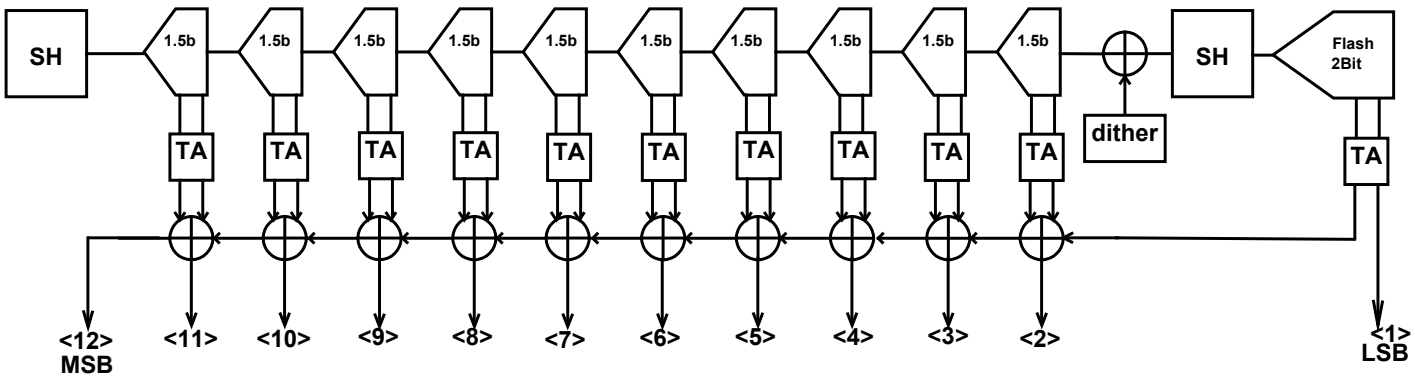
LM-ADC-12B-01 12-bit Pipeline ADC IP Block

Introduction

This document describes the features and key specifications of a 12-bit Pipeline ADC IP block. The process technology for this block is 180 nm CMOS. Modifications to this circuit and different process options are available. Please contact Linear MicroSystems at sales@linearmicrosystems.com for a quotation today.

Features:

- Resolution: 12 bits
- ADC clock input frequency: 60 MHz nominal
- Input full scale signal: 1.6V peak-to-peak differential
- < +/- 1 bit DNL
- < +/- 1 bit INL
- THD @ 10 kHz, -0.5 dB, FS input < 70 dB, FS
- SFDR @ 10 kHz, -0.5 dB, FS input < 70 dB, FS
- 3.3V power supply, 20 mW
- Added analog dither for spur reduction – digital ON/OFF control
- Digital trim capability for improved INL and DNL



Deliverables:

- GDSII + LVS Spice netlist
- User documentation

Ordering Information:

Ordering Part Number	Technology Options	Conditions	Version
LM-ADC-12B-01	180 nm CMOS	0 to 70C	1