

### **LMI101**

# 1553 single channel transceiver with programmable IO characteristics Linear Microsystems, Inc.

# **Product Brief**

#### **OVERVIEW**

The LMI101 single channel transceiver is compliant with 1553/1760 bus transceivers specifications. This transceiver available today in die or optionally in package form or as IP (intellectual property) for integration into mixed signal ASIC designs.

The LMI101 receiver converts 1553 Manchester encoded bi-phase data to complementary TTL (3.3V or 5V) digital outputs. The LMI101 transceiver also provides receiver enable input.

The LMI101 transmitter converts TTL (3.3V or 5V) data to analog bi-phase Manchester data. The 1553 databus transceiver also provides a transmitter enable input.

#### Features:

- 200 kHz to 3 MHz operation
- Single Supply 5V or 3.3V
- Output Driver Withstands Short Circuit Fault
- Outstanding Thermal Impedance Characteristics
- Superior Noise Performance
- Programmable receiver filter
- Programmable receiver FTP (filter output test point) thresholds
- Programmable receiver input comparator low and high thresholds
- Programmable transmit dynamic offset
- Programmable transmit rise time and compensation
- Readback of programmed settings (pretrim)

#### **APPLICATIONS**

- Military and Commercial Avionics
- · Military and Civilian spacecraft on board data handling (OBDH)
- Industrial Control Communications
- Automotive Communications

#### **FUNCTIONAL DESCRIPTION**

The transmitter contains two logic data inputs TXIN L), enable (TXIN H. an (TXENA L), a rise/fall time set circuit, a driver amplifier, an output level control circuit, a master reset (MRST L) and a voltage source push-pull output stage amplifier to drive the center tapped transformer (TXO H/TXO L). The center tap of the transformer is grounded. The receiver has a programmable filter bandwidth and thresholds, high and low.

#### TRANSFORMER

The transformer, (external to this device) which couples the 1553 bus to the ASIC, is center tapped on the ASIC side. The center tap is grounded. The turn's ratio is 1:2.5. The "1" being the center tapped ASIC side of the transformer.

## **OUTPUT AMPLIFIER**

The output amplifier is a voltage source pushpull driver, which provides the output required to drive the center-tapped transformer.

#### RISE/FALL TIME

The nominal rise/fall is 170 ns. Rise/Fall characteristics are adjustable through an I<sup>2</sup>C interface. These settings are static until a Zap operation is performed to lock in the settings permanently.



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#### LOGIC INPUTS

Two logic data inputs are driven by Manchester II encoded logic data. When the transmitter enable is high, the transmitter outputs are in the Hi-Z state, and the two Manchester encoded data inputs are "Don't Care". When the enable is low and the data inputs are in a complementary state, the push-pull output stage provides a balanced drive to the transformer. If both data inputs are logic high or both data inputs are logic low, the transmitter output is put in the Hi-Z state.

#### **PIN LISTING**

NAME	DIR	ACTIVE	PAD	DESCRIPTION
STBY_H	IN, Pullup	High	9	Receive Logic Standby
MRST_L	IN, Pullup	Low	12	Reset transmitter logic
RXENA_H	IN, Pullup	High	8	Receiver enable input high
RXO_H	OUT	High	11	Receiver output high, Manchester II
RXO_L	OUT	Low	10	Receiver output low, Manchester II
RXIN_H	IN	High	3	Receiver input high, Manchester II
RXIN_L	IN	Low	4	Receiver input low, Manchester II
TXO_H	OUT	High	14	Transmitter output high, Manchester II
TXO_L	OUT	Low	2	Transmitter output low, Manchester II
TXIN_H	IN, Pullup	High	15	Transmitter input high, Manchester II
TXIN_L	IN, Pullup	Low	16	Transmitter input low, Manchester II
TXENA_L*	BIDI	Low	13	Transmitter Enable
VADJ	IN	-	6	Voltage Adjustment; varies of TXO_H, L
FTP	OUT	-	5	Filter Test Point
VDD	-	-	1	3.3V or 5V power supply input
VSS	-	-	7	Ground

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# LMI101 BUS Connectivity Example

